Journal of The Electrochemical Society, **146** (9) 3420-3424 (1999)
S0013-4651(98)11-018-2 CCC: $7.00 © The Electrochemical Society, Inc.

Parameter Analysis of Chemical Mechanical Polishing: An Investigation Based on the Pattern Planarization Model

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Based on the pattern planarization model, polishing time, polished thickness, and the planarization efficiency of a point of interest on a wafer during the chemical mechanical process are expressed as functions of polishing parameters. The influences as well as the variation of polishing time, polished thickness, and planarization efficiency across the wafer are also presented. Polished thickness uniformity and planarization uniformity are also presented. The effects of polishing parameters on the process are discussed and the predicted trends in adjusting these polishing parameters are illustrated.
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Manuscript submitted November 3, 1998; revised manuscript received May 7, 1999.

The ability for local and global planarization is becoming important as the desired feature sizes of semiconductor wafers continue to shrink. Of all the planarization technologies, chemical mechanical polishing (CMP) is the most effective planarization technology for achieving smaller feature size and multilevel interconnections for the integrated circuit (IC) industry.[1-3] CMP is used to polish interlevel dielectrics and metal films in general and can be extended to many planarization techniques in device fabrication.[4,5]

The polishing mechanism, process control, and basic understanding of CMP remain essentially on the experiential level. There is a variety of physical and chemical effects that are involved in the CMP process, and analysis from several scientific and engineering fields are needed.[6] Slurry composition, the size of slurry particles, flow rate, and the direction of slurry impingement onto the polishing pad play important roles in the chemical process. The mechanical process is affected by applied pressure, rotational speeds of the pad and wafer, density and viscosity of the slurry, and the material and surface microstructures of the pad and carrier film. The Preston equation,[6] an empirical equation for glass polishing, describes the mechanical removal rate as a function of applied pressure and the relative speed between the substrate and the polishing pad. Runnels and Eyman[8] proposed a model accounting for stress in the polishing pad and fluid flow, as well as the removal of material by erosion. Based on statistical method and elastic theory, Liu *et al.*[9] showed that the mechanical removal rate is dependent on the elastic modulus of the slurry particles and polished film. Tseng and Wang[10] modified the Preston equation and showed that the mechanical removal rate is proportional to the applied pressure to the $^5/_6$ order and the polishing velocity to the $^1/_2$ order. Wang *et al.*[11] showed that Von Mises stress correlates with polishing nonuniformity while normal stress does not, and uniformity can be improved by decreasing polishing pad and carrier film compressibility. Based on contact mechanics, Chekina *et al.*[12] developed a wear-contact model of the CMP process which includes parameters such as pad deformation and wafer surface evolution. Chen and Lee[13] developed a polishing model that considers the patterns on the wafer. Time-dependent removal rate is presented to describe the planarization of patterns.

In the following, a polishing model considering the patterns on the wafer surface[13] is adopted whereby the influences of process variables such as polishing time, polished thickness, and planarization efficiency at a point of interest can be obtained. The variation of polishing velocity, polishing time, and polished thickness across the wafer are also shown. The relations between uniformity of global planarization and polishing parameters such as angular velocity ratio of carrier and pad, applied pressure, and pad material are presented. The effects of variation of the polishing parameters are summarized and the predicted trends in adjusting the polishing parameters are illustrated.

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Pattern Planarization Model

Figure 1 shows a schematic diagram of the CMP configuration. The wafer is mounted upside down on the wafer carrier and rotates above a pad sitting on a table. The slurry that flows between the wafer and the pad dissolves and removes the wafer layer. An initial step height, h_0, between the upper and lower feature surfaces is shown in Fig. 2a. The polished thickness on upper and lower feature surfaces, δ_U and δ_L, are shown in Fig. 2b. In the following, polishing behavior with the existence of pattern is considered with the following assumptions[13]

1. Material removal is anisotropic downward and has no effect on the sidewall of the profiles.

2. The pressures on the upper and lower surfaces, P_U and P_L, are proportional to the step height, h, *i.e.*

$$P_U - P_L = \alpha h \qquad [1]$$

where the loading density coefficient, α, indicates stiffness of the polishing pad.

3. The polishing mechanism at every point on the wafer follows the linear wear equation.[14]

From the assumptions, Chen and Lee[13] showed that the removal rate of the upper feature surface, $\dot{\delta}_U$, the removal rate of the lower feature surface, $\dot{\delta}_L$, and the normalized step height, h_n, can be written as

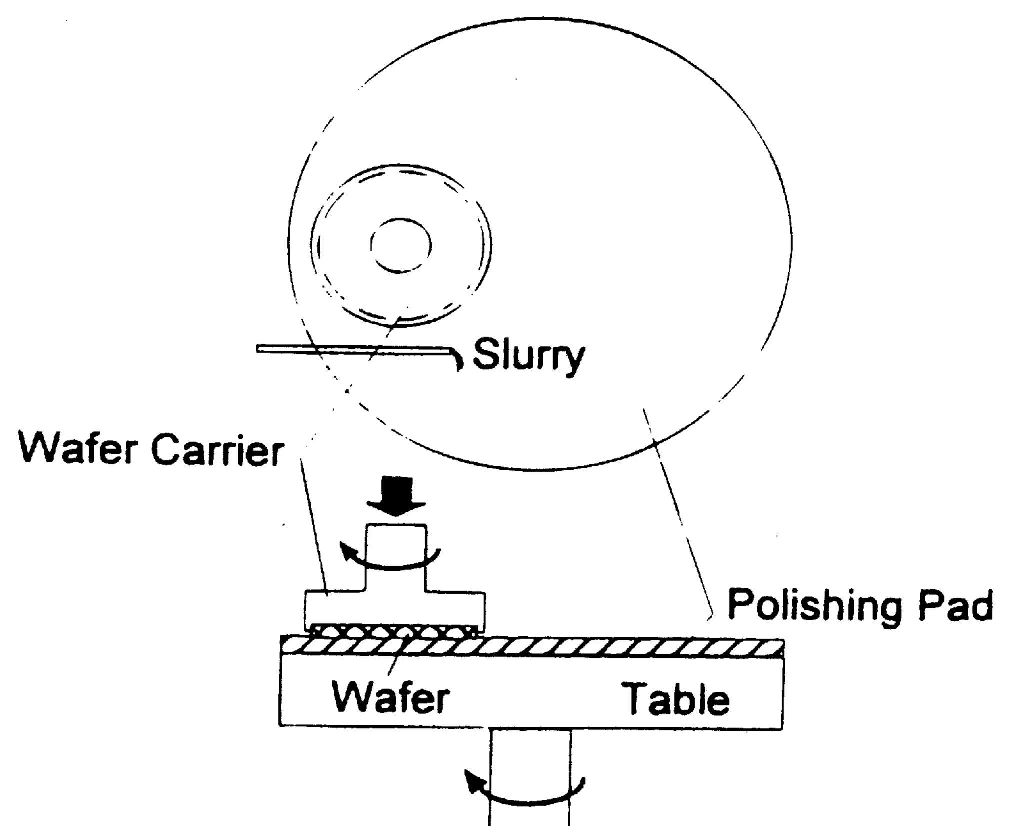

Figure 1. Schematic diagram of CMP polisher.

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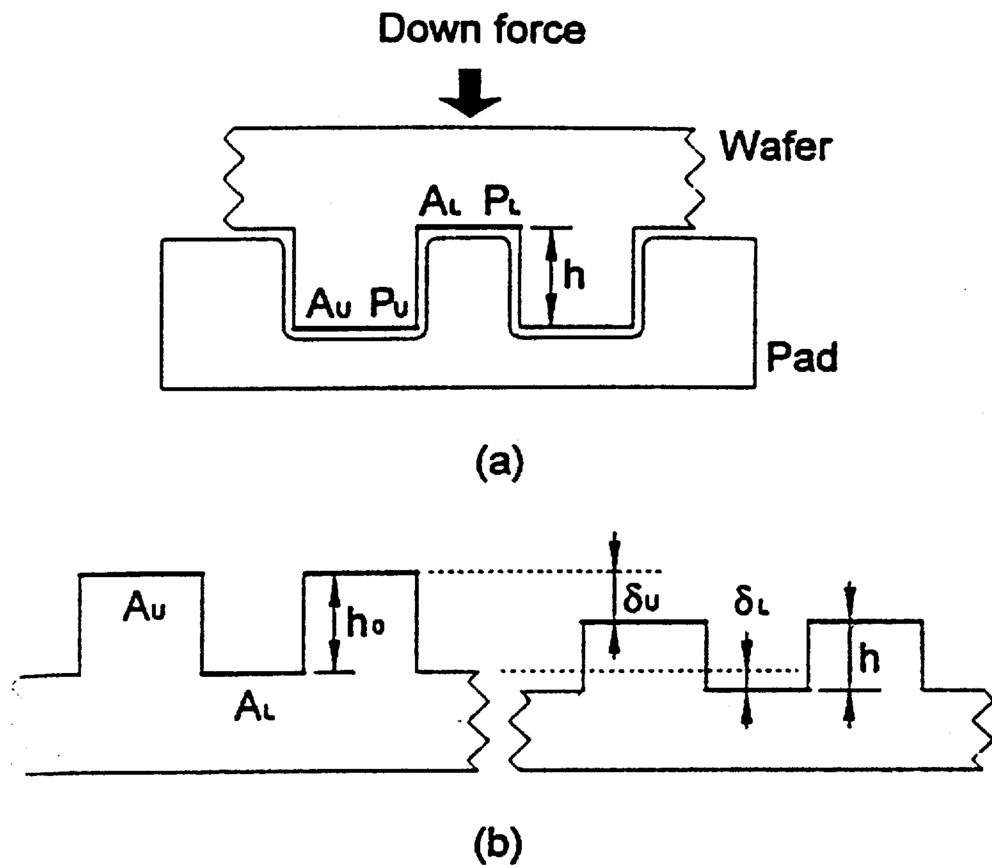

Figure 2. (a) Cross section of the patterns and pad profiles. (b) Patterns before and after polishing.

$$\dot{\delta}_U = \frac{K}{H}V\left[P + (1 - D)\alpha h_0 \exp\left(-\frac{K}{H}V\alpha t\right)\right] \quad [2]$$

$$\dot{\delta}_L = \frac{K}{H}V\left[P - D\alpha h_0 \exp\left(-\frac{K}{H}V\alpha t\right)\right] \quad [3]$$

$$h_n = \frac{h}{h_0} = \exp\left(-\frac{1}{H}KVt\right) \quad [4]$$

where P is the applied pressure, V the polishing velocity, H the hardness of pad material, D the pattern density defined as the ratio of upper feature surface to the total area, h_0 is the initial step height, and the wear coefficient, K, is

$$K = 24.72P^{0.3}\dot{\theta}_1^{-0.79}k_v^{-0.14} \quad [5]$$

and where k_v is the ratio between the angular velocity of the wafer, ω_w, and the table, ω_t, and

$$\dot{\theta}_1 = -\omega_t \quad [6]$$

Let a_1 be the offset distance between centers of the table and the wafer and a_2 be the distance of the wafer center to a point of interest. Chen and Lee[13] showed that the polishing velocity, V, can be written as

$$V = \frac{2}{\pi}\left|\dot{\theta}_1(a_1 + a_2 - k_v a_2)\right|E(m) \quad [7]$$

where

$$E(m) = \int_0^{\pi/2}(1 - m\sin^2\theta)^{1/2}d\theta \quad [8]$$

and

$$m = \frac{4a_1a_2(1 - k_v)}{(a_1 + a_2 - k_v a_2)^2} \quad [9]$$

Variation of polishing velocity.—From Eq. 7, it can be seen that the polishing velocity is a function of the distance between the centers of the table and wafer, the distance between the wafer center to the point of interest, and the relative angular velocity of table and wafer. From Eq. 7, the polishing velocity at wafer center, V_0, can be written as

$$V_0 = a_1|\dot{\theta}_1| \quad [10]$$

In order to represent the diversity of polishing velocity, the center of the wafer is chosen as a reference point since its polishing velocity is independent of the angular velocity ratio. Let R_v be the polishing velocity ratio between a point of interest to the wafer center. The polishing velocity can then be written as

$$R_v = \frac{V}{V_0} \quad [11]$$

Let the position ratio, r, be defined as

$$r = \frac{a_2}{a_1} \quad [12]$$

From Eq. 7-12, the polishing velocity ratio, R_v, can be written as

$$R_v = \frac{2}{\pi}\left|1 + r - rk_v\right|E(m) \quad [13]$$

Figure 3 shows the polishing velocity ratio *vs.* position ratio for various angular velocity ratios. It can be seen that the polishing velocity ratio is constant when the angular velocity ratio is 1. Hence, every point on the wafer has the same polishing velocity while the angular velocities of table and carrier are equal.

Polishing Time

The depth of focus for lithography systems is shrinking rapidly and pushing the wafer-surface topography beyond depth-of-focus capability. A limited step height, h, is desired to prevent the wafer surface topography from exceeding the depth of focus. With a given initial step height, h_0, which is determined by the wafer surface topography before the CMP process, the requirement of planarization can be defined as the ratio of the limited step height for depth of focus, h, to the initial step height, h_0. Hence, the normalized step height, h_n, can be used to specify the requirement of planarization. From Eq. 4, the polishing time can be obtained as

$$t = -\frac{H}{\alpha(KV)}\ln(h_n) \quad [14]$$

Equation 14 shows that the polishing time can be determined for given polishing conditions with a specified requirement of planarization, h_n, while suitable polishing conditions may be obtained from the "KV" term for a specified polishing time and h_n. Note that the KV term can be evaluated from Eq. 5 and 7 with specified applied pressure, angular velocities of table and carrier, offset distance between the centers of pad and wafer, and distance between the wafer center to the point of interest. Figure 4 shows the position-dependent KV *vs.* the angular velocity ratio, k_v, at various table speeds with a_1 = 20 cm, a_2 = 10 cm, and P = 7 psi. Figure 5 shows the variation of polishing time *vs.* the requirement of planarization h_n of a

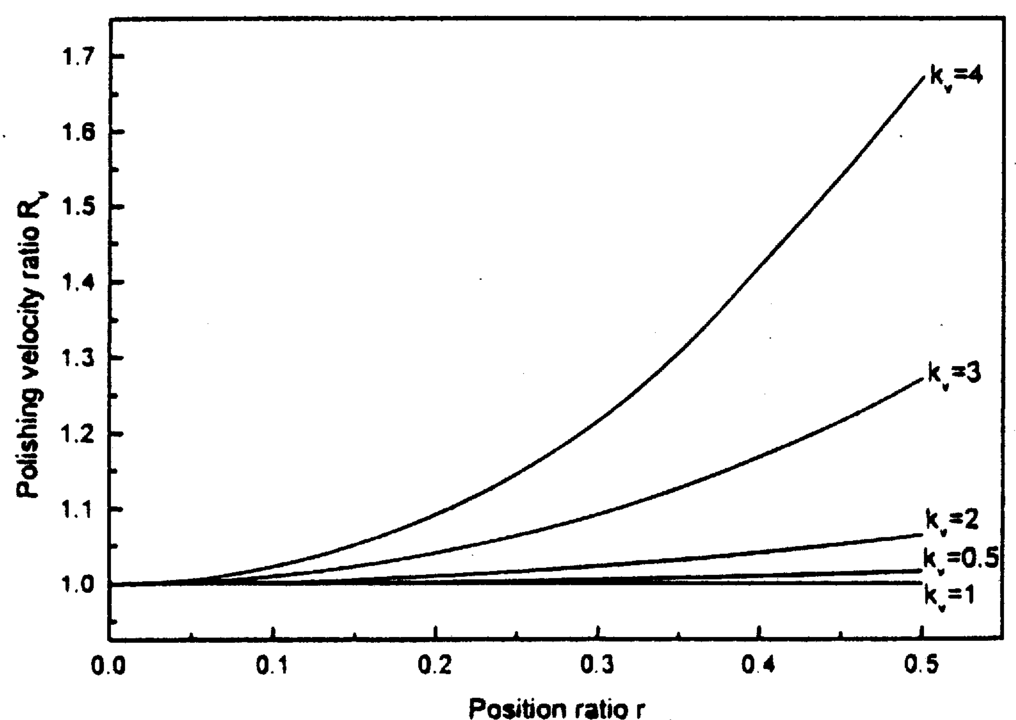

Figure 3. R_v *vs.* r at various angular velocity ratios.

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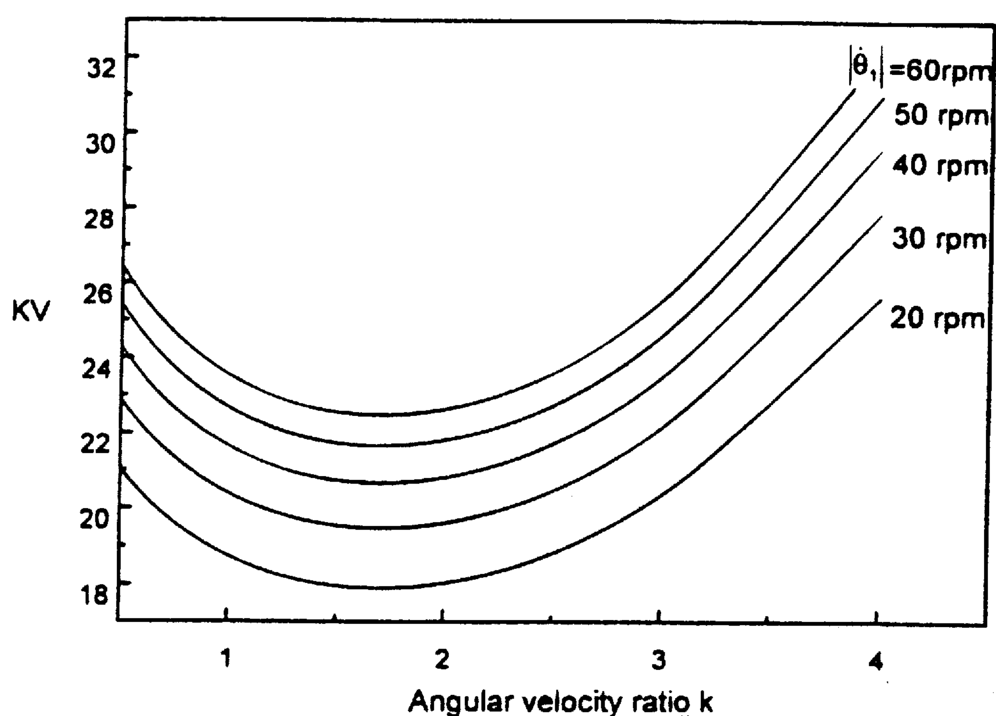

Figure 4. "KV" *vs.* k_v at various table speeds (a_1 = 20 cm and a_2 = 10 cm).

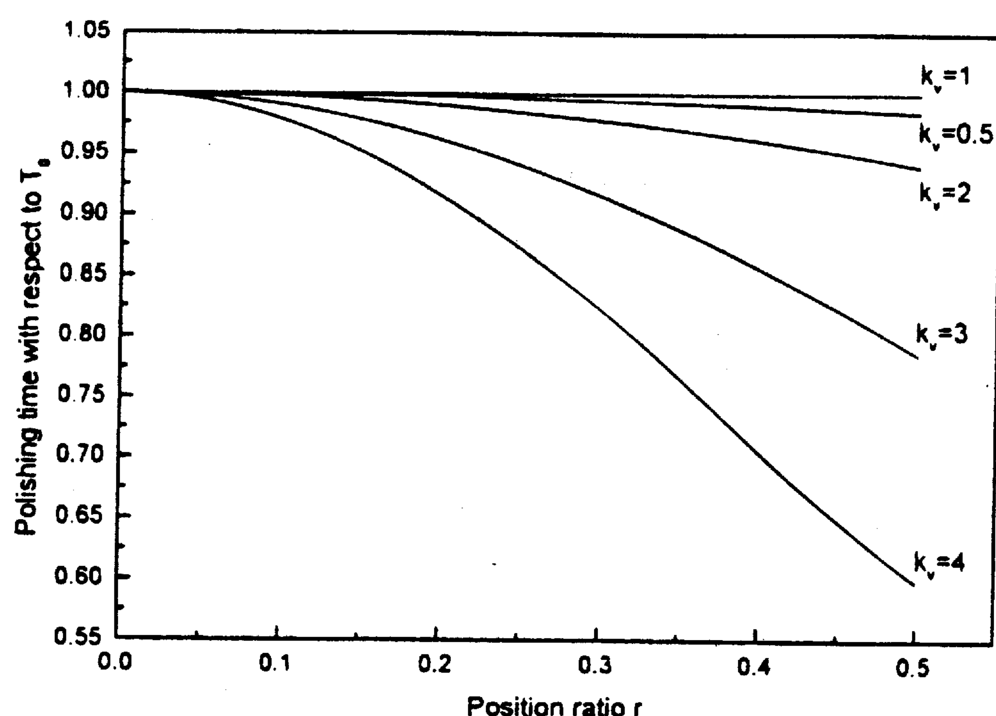

Figure 6. t/T_0 *vs.* r at various angular velocity ratios (P = 7 psi and H = 0.8).

TEOS film (H = 0.8 and α = 0.7974 Tpa/m).[13] From Fig. 5 it can be seen that the polishing time increases rapidly while the requirement of planarization is increased.

Variation of polishing time.—From Eq. 14, it can be seen that the polishing time varies from point to point due to the position-dependent polishing velocity. Assuming the polishing conditions such as the pad condition, pad hardness, loading coefficient, and wear coefficient across the entire wafer remain stable, then from Eq. 14 polishing time at the wafer center, T_0, can be written as

$$T_0 = -\frac{H}{KV_0\alpha}\ln(h_n) \qquad [15]$$

Let the polishing time for planarization on the wafer center point be T_0. The polishing time with respect to T_0 to reach the requirement of planarization can be obtained as

$$\frac{t}{T_0} = \frac{1}{R_v} \qquad [16]$$

From Eq. 11 and 16, it can be seen that the polishing time with respect to T_0 is a function of the position ratio and the angular velocity ratio. Figure 6 shows the polishing time with respect to T_0 *vs.* the position ratio for polishing a tetraethoxysilane (TEOS) film with applied pressure of 7 psi at various angular velocity ratios.

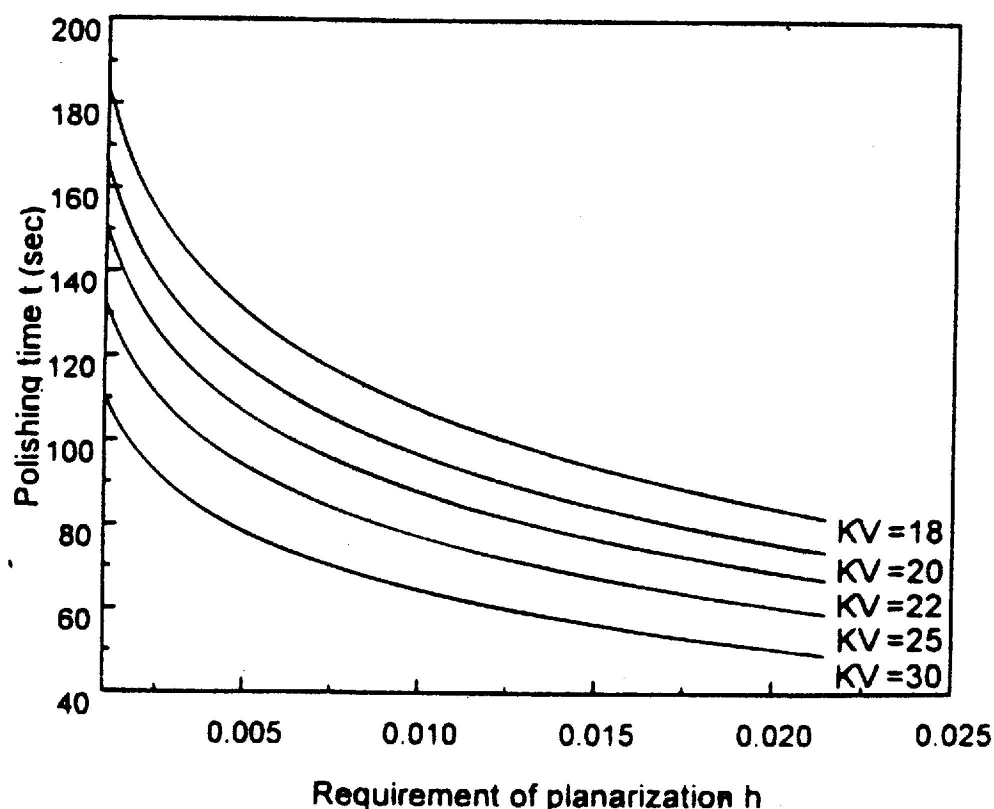

Figure 5. t *vs.* h_n at various "KV" (H = 0.8).

Polished Thickness

For dielectric polishing, the goal is to remove topography and maintain good uniformity across the entire wafer. The polished thickness can provide a reference deposition thickness to the chemical vapor deposition (CVD) process before CMP. The polished thickness for planarization at the upper feature surface, δ_U, and lower feature surface, δ_L, can be obtained by integrating Eq. 2 and 3 as

$$\delta_U = \frac{K}{H}PVt + h_0(1 - D)\left[1 - \exp\left(-\frac{K}{H}V\alpha t\right)\right] \qquad [17]$$

and

$$\delta_L = \frac{K}{H}PVt - h_0D\left[1 - \exp\left(-\frac{K}{H}V\alpha t\right)\right] \qquad [18]$$

Equations 17 and 18 show that the polished thickness on the upper and lower feature surfaces can be determined with specified applied pressure, pattern density, initial step height, stiffness of pad material, and polishing velocity. By substituting Eq. 4 into Eq. 17 and 18, we have

$$\delta_U = -\frac{P}{\alpha}\ln(h_n) + h_0(1 - D)[1 - h_n] \qquad [19]$$

and

$$\delta_L = -\frac{P}{\alpha}\ln(h_n) - h_0D[1 - h_n] \qquad [20]$$

Equations 19 and 20 show that the polished thickness on the upper and lower feature surfaces can be determined for a given requirement of planarization, h_n, with specified applied pressure, pattern density, and initial step height. From Eq. 19 and 20, it can be seen that a higher applied pressure increases the polished thickness on the upper and lower feature surfaces. Figures 7 and 8 show the normalized step height *vs.* polished thickness on the upper and lower feature surfaces of a polished TEOS film (H = 0.8 and α = 0.7974 Tpa/m) [13] with initial step height 7000 Å and pattern density of 0.1 at various applied pressures.

Variation of polished thickness.—For a given polishing time, the polished thickness on the upper and lower feature surfaces can be obtained from Eq. 19 and 20 by substituting the evaluated normal step height at a point of interest on the wafer. Figures 9 and 10 show the polished thickness on the upper and lower feature surfaces *vs.* the position ratio for polishing a TEOS-covered wafer with P = 7 psi, ω_t = 20 rpm, D = 0.1, and polishing time of 60 s at various polishing velocity ratios. From Fig. 9 and 10 it can be seen that the feature

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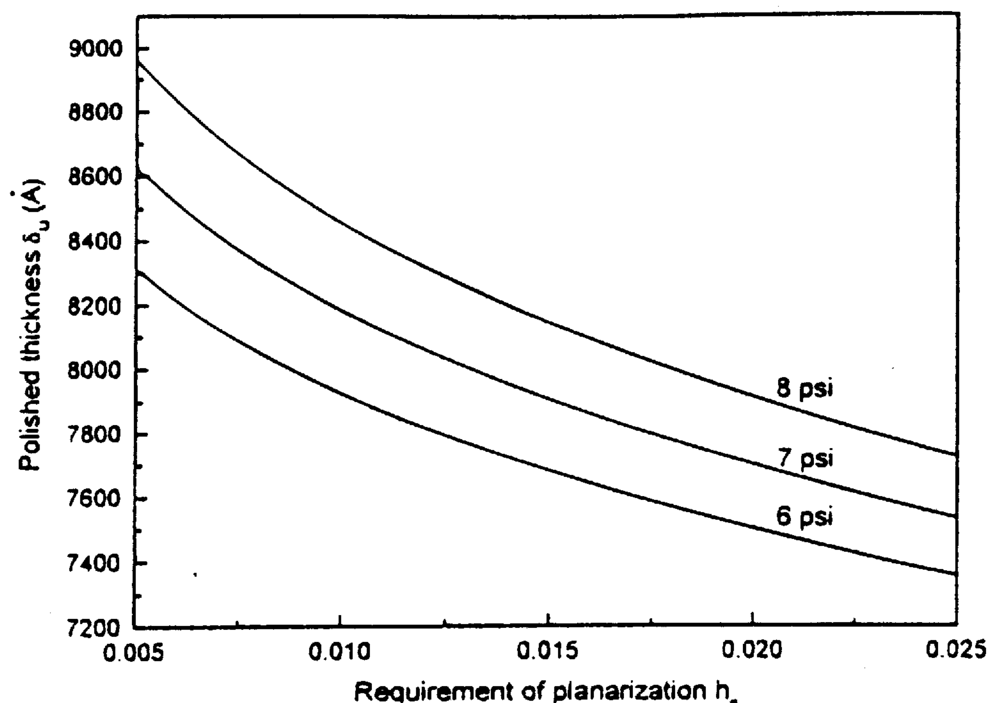

Figure 7. δ_U *vs.* h_n at various applied pressures (h_0 = 7000 Å and D = 0.1).

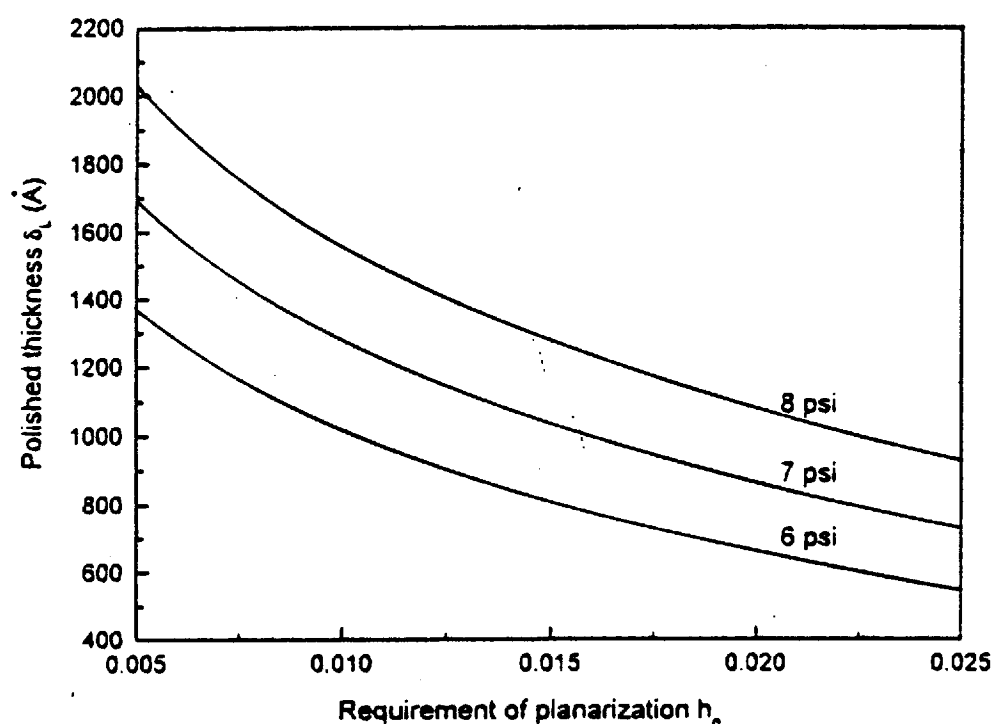

Figure 8. δ_L *vs.* h_n at various applied pressures. (h_0 = 7000 Å and D = 0.1.)

surface polished thickness is about 267 Å at the center of the wafer and about 700 Å at the edge.

Two issues can be used to evaluate the result of CMP in the viewpoint of global planarization. One is the uniformity of polished thickness within the wafer and the other is the uniformity of planarization within the wafer. The polished thickness uniformity, PTU, which estimates the material removal difference within the wafer, can be defined as

$$\mathrm{PTU} = \frac{\delta_{U,\max} - \delta_{U,\min}}{2\bar{\delta}_U} \quad [21]$$

where $\bar{\delta}_U$ is the average polished thickness of measured points.[15]

From this definition, the lower the PTU, the better the uniformity. From Fig. 9 and 10, it can be seen that the maximum polished thickness lies at the wafer edge and the minimum polished thickness lies at the wafer center. Figure 11 shows the PTU *vs.* angular velocity for polishing a TEOS-covered wafer at different applied pressures with ω_t = 20 rpm, D = 0.1, and t = 60 s at various applied pressures.

The planarization uniformity, PU, which indicates the planarity within the wafer, can be defined as

$$\mathrm{PU} = \frac{h_{\max} - h_{\min}}{2\bar{h}} \quad [22]$$

where $\bar{h}$ is the average step height of measured points.[16]

From the definition, the lower PU, the better the planarity. The maximum step height is at the wafer edge, and the minimum step height is at the wafer center theoretically. Figure 12 shows the PU *vs.* the angular velocity ratios for polishing a TEOS-covered wafer with ω_t = 20 rpm, D = 0.1, and t = 60 s at various applied pressures.

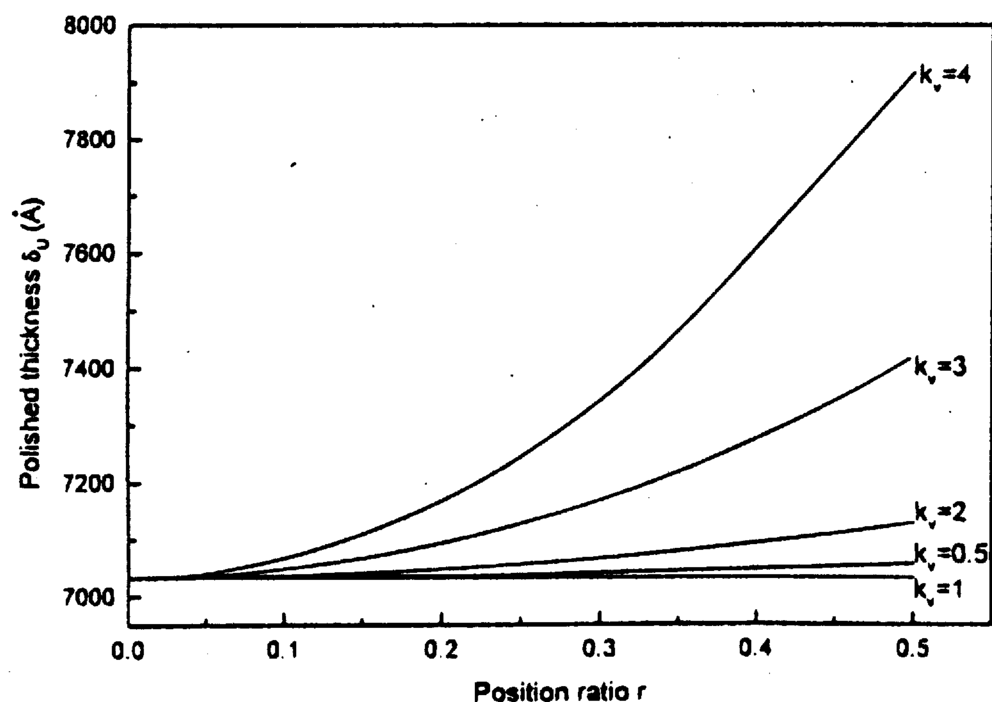

Figure 9. δ_U *vs.* r at various angular velocity ratios (h_0 = 7000, $\dot{\theta}_l$ = 20 rpm, P = 7 psi, t = 60 s, H = 0.8, and D = 0.1).

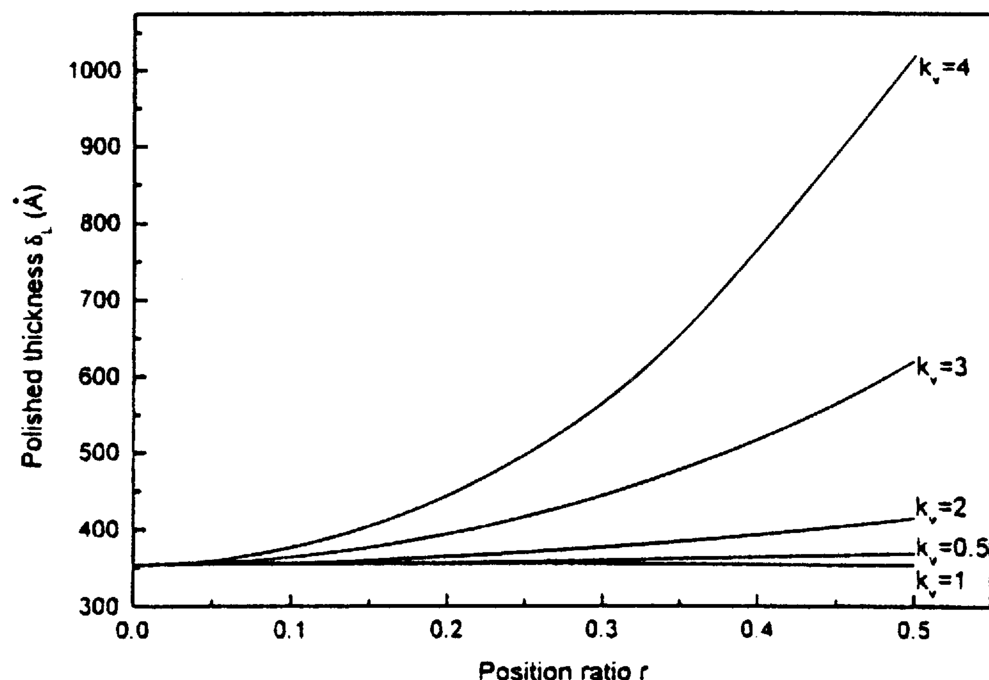

Figure 10. δ_L *vs.* r at various angular velocity ratios (h_0 = 7000 Å, $\dot{\theta}_l$ = 20 rpm, P = 7 psi, t = 60 s, H = 0.8, and D = 0.1).

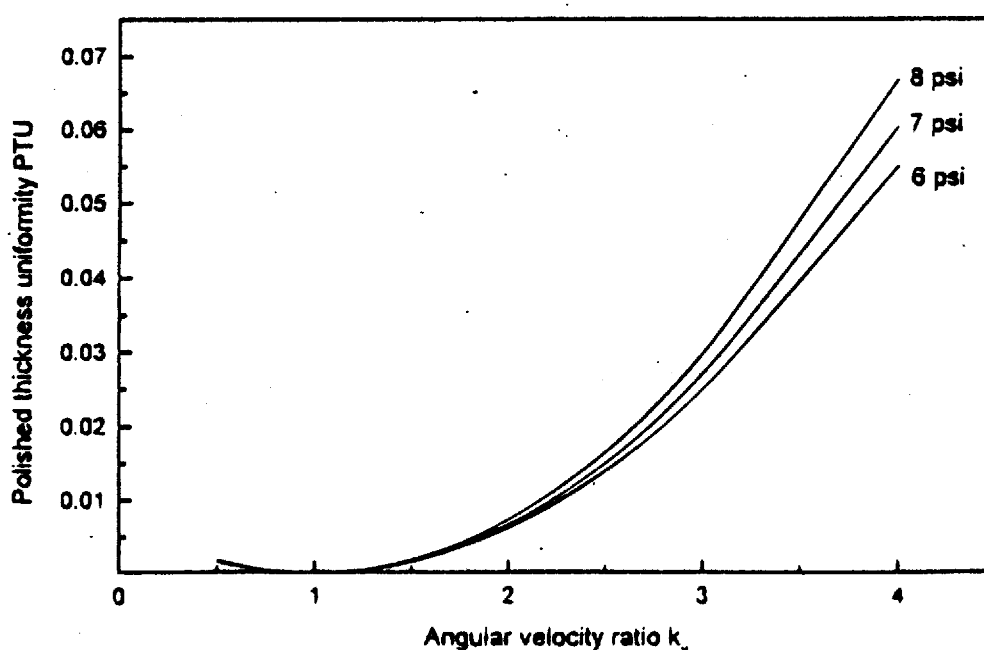

Figure 11. PTU *vs.* k_v at various applied pressures ($\dot{\theta}_l$ = 20 rpm, D = 0.1, t = 60 s, and H = 0.8).

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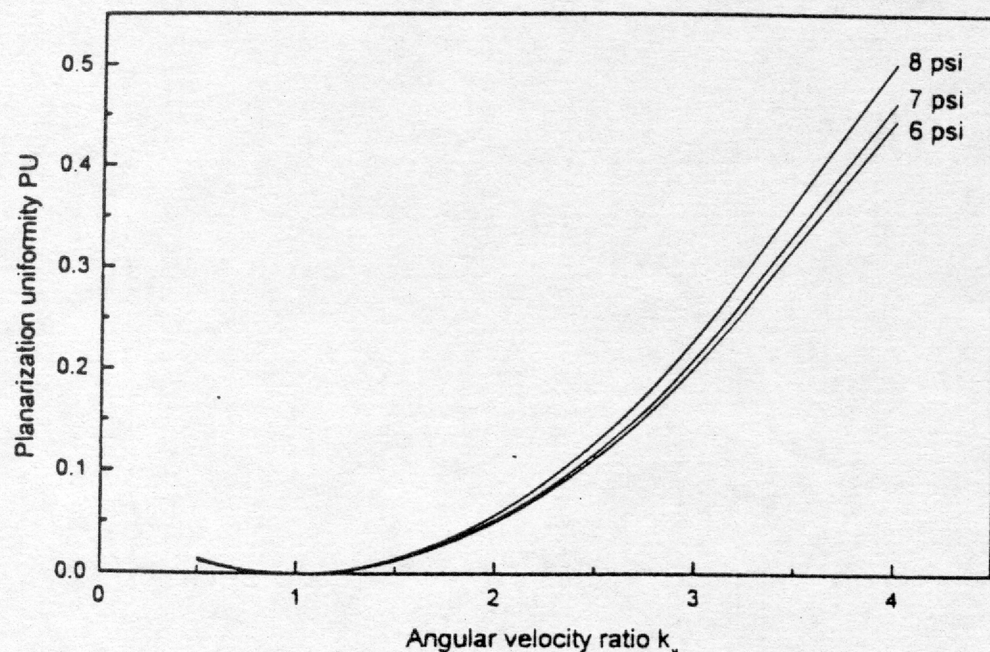

Figure 12. PU *vs.* k_v at various applied pressures ($\dot{\theta}_1$ = 20 rpm, D = 0.1, t = 60 s, and H = 0.8).

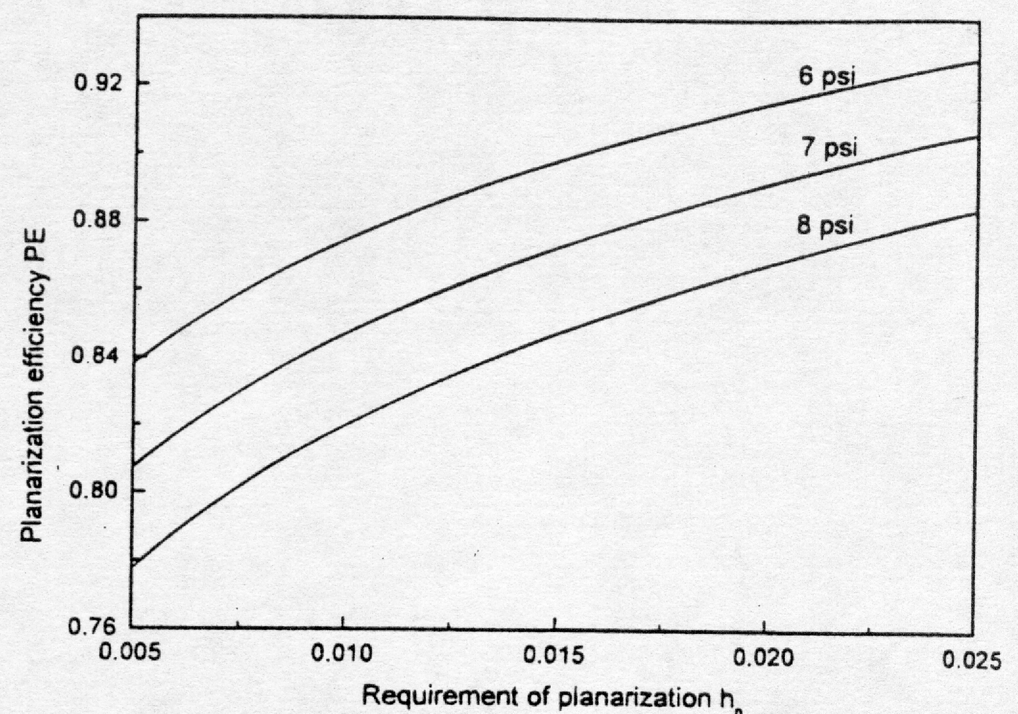

Figure 13. PE *vs.* h_n at various applied pressures (h_0 = 7000 Å and D = 0.1).

Planarization Efficiency

The polishing action progresses in both upper and lower feature surfaces of the wafer. The most efficient method in planarization is to remove the upper features only, but this is difficult in a real polishing process. The planarization efficiency, PE, which indicates the efficiency of the CMP process, can be defined as

$$PE = 1 - \frac{\Delta Down}{\Delta Up} = 1 - \frac{\delta_L}{\delta_U} \quad [23]$$

By substituting Eq. 19 and 20 into Eq. 23, PE can be rewritten as

$$PE = \frac{h_0[1 - h_n]}{-P/\alpha \ \ln(h_n) + h_0(1 - D)[1 - h_n]} \quad [24]$$

Equation 24 shows that PE can be evaluated for a given h_n, applied pressure, pattern density, initial step height, and load density. From Eq. 24, it can be seen that PE can be improved with a lower applied pressure. Figure 13 shows the normalized step height *vs.* PE for various pressures with h_0 = 7000 Å and D = 0.1.

Conclusion

Improvement of CMP process performance is foremost for CMP application. In general, adjustment of the process parameters is achieved empirically. However, there are numerous variables in the CMP process and the relations between these variables are complex. There are several parameters that are indeed influential on the CMP process, such as applied pressure, rotational speeds of the carrier and table, etc. Each parameter is capable of affecting CMP performance in various ways.

From Fig. 7 and 8 it can be seen that increasing applied pressure increases the polished thickness on the upper and lower feature surfaces. From Fig. 13 it can be seen that planarization efficiency can be increased under a higher pressure. Both the PU and PTU decrease while the pressure on the wafer increases.

The angular velocity ratio is important to the control of CMP performance. The higher angular velocity ratio reduces the normalized step height for a given polishing time. This causes the polished thickness on the upper and lower feature surfaces to increase and the planarization efficiency to decrease. Figure 6 shows that a large value of angular velocity ratio causes great variation of polishing time at various points across the wafer. Figures 11 and 12 show that the angular velocity ratio also causes degradation of uniformity both of the PU and the PTU. Note that uniformity improves as the angular velocity ratio approaches 1.

National Taiwan University assisted in meeting the publication costs of this article.

References

1. K. Skidmore, *Semicond. Int.*, 115 (1988).
2. F. Malik and R. Solanki, *Thin Solid Films*, **193**, 1030 (1990).
3. M. A. Martines, *Solid State Technol.*, 26 (1994).
4. J. Warnock, *J. Electrochem. Soc.*, **138**, 2398 (1991).
5. F. B. Kaufman, D. B. Thompson, R. E. Broadie, M. A. Jaso, W. L. Guthrie, D. J. Pearson, and M. B. Small, *J. Electrochem. Soc.*, **138**, 3460 (1991).
6. I. Ali, S. R. Roy, and G. Shinn, *Solid State Technol.*, 63 (1994).
7. F. W. Preston, *J. Soc. Glass Technol.*, **11**, 214 (1927).
8. S. R. Runnels and L. M. Eyman, *J. Electrochem. Soc.*, **141**, 1698 (1994).
9. C. W. Liu, B. T. Dai, W. T. Tseng, and C. F. Yeh, *J. Electrochem. Soc.*, **143**, 716 (1996).
10. W. T. Tseng and Y. L. Wang, *J. Electrochem. Soc.*, **144**, L15 (1997).
11. D. Wang, J. Lee, K. Holland, T. Bibby, S. Beaudioin, and T. Cale, *J. Electrochem. Soc.*, **144**, 1121 (1997).
12. O. G. Chekina, L. M. Keer, and H. Liang, *J. Electrochem. Soc.*, **145**, 2210 (1998).
13. D. Z. Chen and B. S. Lee, *J. Electrochem. Soc.*, **146**, 744 (1999).
14. D. A. Rigney, *Wear*, **175**, 63 (1994).
15. R. Kolenkow and R. Nagahara, *Solid State Technol.*, 114 (1992).
16. P. Renteln, M. Thomas, and J., Pierce, in *Proceedings of the 7th International VLSI Multilevel Interconnection Conference*, VMIC, p. 57, Piscataway, NJ (1990).